SOLE INVENTOR

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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Young-Min KWON**, a citizen of Korea, residing at 891-10, Daechi-dong, Kangnam-ku, Seoul, 135-523, Korea, have invented a new and useful SEMICONDUCTOR DEVICE AND A FABRICATION METHOD THEREOF, of which the following is a specification.

SEMICONDUCTOR DEVICE AND A FABRICATION METHOD THEREOF

TECHNICAL FIELD

[0001] The present disclosure relates to a semiconductor device and a fabrication method thereof and, more particularly, to a photolithography process using a far ultraviolet ray.

BACKGROUND

[0002] Recently, because of the development of integration, it is now practical to use large scale integration ("LSI") and very large scale integration ("VLSI") in the fabrication of semiconductor integrated circuits. Furthermore, the minimum pattern of integrated circuit is now at a sub-micron scale, which tends to be a more fine scale one.

[0003] In order to form a micro pattern, it is essential to use a photolithography technique in which a photoresist layer is formed on a substrate on which a thin film will be formed, a selective exposure is performed to form a latent image of a desired pattern, a photoresist pattern is made by development, the thin film is etched using the photoresist pattern as a mask, and the desired pattern of the thin film is obtained by removing the photoresist pattern.

[0004] Although an ultraviolet ray such as a G-ray (wavelength 436nm) or an I-ray (wavelength 365nm) is typically used as the exposure light source in the photolithography technique, a far ultraviolet ray (wavelength 248nm) with shorter wavelength is used for finer patterns.

[0005] Now, a conventional photolithography process using a far ultraviolet ray to form a metal layer pattern is described.

[0006] First, an interlayer insulating layer is formed on a structure of semiconductor substrate, i.e., a semiconductor substrate on which a device unit is formed, or a metal line layer, and a metal layer is formed on the interlayer insulating layer.

[0007] Next, a metal pattern to form a semiconductor device circuit is formed by the following process: 250Å of an anti-reflection layer is formed on the metal layer; 50Å of a protective oxide layer is formed on the anti-reflection layer; a photoresist layer for a far ultraviolet ray is applied, exposed, and developed to form a photoresist pattern; the exposed metal layer is etched using the photoresist pattern as a mask and the far ultraviolet ray as a light source.

[0008] At this time, the protective oxide layer is selectively formed. In Fig. 1, an example that an anti-reflection layer 2 is formed on a metal layer 1, on which a photoresist layer 3 is applied using the above conventional method, is shown. In this example, it is not unusual that the photoresist pattern is lifted because the contact layer between the photoresist layer 3 and anti-reflection layer 2 is smooth, which may result in a defective metal pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 is a cross sectional view showing an example structure having an anti-reflection layer formed on a metal layer and a photoresist layer applied thereon according to a conventional method.

[0010] Fig. 2 is a cross sectional view showing another example structure having an anti-reflection layer formed on a metal layer and a photoresist layer applied thereon.

[0011] Figs. 3A and 3B are cross sectional views showing example structures having an anti-reflection layer and a protective oxide layer formed on a metal layer in order and a photoresist layer is applied thereon.

DETAILED DESCRIPTION

[0012] A fabricating method of a semiconductor device may include forming a film which is an object of forming a pattern on a structure of a semiconductor substrate; forming a anti-reflection layer on the film to form a stacking structure including the film and the anti-reflection layer; performing a plasma treatment to form grooves on a upper surface of the stacking structure; forming a photoresist pattern on the stacking structure on which the grooves are formed; and etching the stacking structure using the photoresist pattern as a mask to form a stacking structure pattern.

[0013] It is preferable that the plasma treatment is performed for 15-30 seconds using N_2O plasma.

[0014] Forming the photoresit pattern on the stacking structure may include applying a photoresist layer, exposing the photoresist layer to a light selectively, and developing the photoresist layer to form the photoresist pattern exposing a part of the stacking structure. In exposing the photoresist layer to a light selectively, a far ultraviolet ray may be used as a light source.

[0015] A SiOxNy layer having thickness of 200~300Å can be used as the anti-reflection layer and the film is preferably a metal film.

[0016] During the stacking structure formation, a protective oxide layer may be formed on the anti-reflection layer after forming the anti-reflection layer to form a stacking structure including the film, the anti-reflection layer, and the protective oxide layer.

[0017] It is preferable that the protective oxide layer is formed to have thickness of equal to or less than 100Å.

[0018] As described in greater detail below, the example semiconductor devices and fabrication method thereof described herein prevent the lift phenomenon of a photoresist pattern.

[0019] In particular, an anti-reflection layer and/or a protective oxide layer is formed on a film which is an object of pattern formation, N_2O plasma treatment is performed to form grooves thereon, and a photoresist layer is applied thereon thereby improving adhesiveness between the photoresist layer and anti-reflection layer/protective oxide layer.

[0020] An example fabrication method that may be used to form the example semiconductor device described herein is described below in detail with reference to accompanying drawings.

[0021] First, an interlayer insulating layer is formed on a structure of semiconductor substrate, i.e., a semiconductor substrate on which a device unit is formed, or a metal line layer, and a metal layer is formed on the interlayer insulating layer. Next, an anti-reflection layer is formed on the metal layer to reduce the reflectivity of the metal layer, where 200~300Å of SiOxNy is used as the anti-reflection layer. Then, N_2O plasma treatment is performed on the anti-reflection layer to form grooves. It is preferable to perform the N_2O plasma treatment for 15-30 seconds. When the photoresist layer is applied after forming the grooves on the anti-reflection layer, there is an advantage that the adhesiveness between the anti-reflection layer and the photoresist layer is much improved. Then, a metal pattern is formed by the following process: a photoresist pattern, which partially exposes the metal layer, is formed by applying photoresist on

the anti-reflection layer, selective exposure, and development; the exposed metal layer is etched using the photoresist pattern as a mask.

[0022] As shown in Fig. 2, a first example semiconductor device includes an anti-reflection layer 12 formed on a metal layer 11 on which the photoresist layer 20 is formed. Grooves are formed on the anti-reflection layer 12 which locates below the photoresist layer 20.

[0023] However, a footing phenomenon, i.e., the photoresist is not completely removed and remains due to the reaction between the anti-reflection layer and the amine radical of the far ultra-violet, the exposure light, occurs frequently. The protective oxide layer may be formed on the anti-reflection layer to prevent the footing phenomenon.

[0024] The protective oxide layer is preferably formed with thickness of equal to or less than 100Å and 50Å.

[0025] Another example semiconductor device where a protective oxide layer is formed is shown in Fig. 3A. In Fig. 3A, an example where the anti-reflection layer 12 and the protective oxide layer 13 are applied in order on the metal layer 11, on which the photoresist layer 20 is applied is shown, where the grooves are formed on the protective oxide layer 13. However, the plasma treatment can make the grooves not only on the protective oxide layer 13 but also on the anti-reflection layer 12 beneath the protective oxide layer.

[0026] Yet another example semiconductor device where the grooves are formed on the anti-reflection layer 12 is shown in Fig. 3B. In Fig. 3B, an example where the anti-reflection layer 12 and the protective oxide layer 13 are applied in order on the metal layer 11, on which the photoresist layer 20 is applied is shown, where the grooves are formed on the protective oxide layer 13 and the anti-reflection layer 12.

[0027] As detailed above, there is an effect of preventing the phenomena that the photoresist layer pattern is lifted after the development because the adhesiveness between the anti-reflection layer or the protective oxide layer and the photoresist layer is enhanced through the following process that the grooves are formed on either the anti-reflection layer or the protective oxide layer, or both of them, by performing the N_2O plasma treatment before applying the photoresist layer.

[0028] While the examples herein have been described in detail with reference to example embodiments, it is to be understood that the coverage of this patent is not

limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the sprit and scope of the appended claims.